#8 Suppl. Decl. W/Patent 8-5-98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Vora

Art Unit:

Examiner:

Serial No. 08/654,760

Filed: 5/29/96

For: VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COST

Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
June 9, 1998

NOA containing Sub

DECLARATION OF MADHUKAR VORA UNDER 37 CFR 1.132

Dear Sir:

Being hereby warned that any false statements and the like herein are punishable by fine or imprisonment (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon, the undersigned hereby declares that all statements herein are made of the declarants own knowledge and are true, and any statements made on information and belief are believed to be true.

I, Madhukar Vora, am the inventor of the claimed subject matter in the above identified patent application. I was born in 1938 and have a Master of Science in Electrical Engineering from Worcester Polytechnic Institute in Worcester, Mass. I was a device engineering manager at IBM from 1962 to 1973 where I filed and received a large number of patents on semiconductor device structures and circuits. From 1973 to 1987, I was Director of R&D at the Palo Alto Research Center of Fairchild Camera and Instrument, Inc. where I filed and

receiv d a larg number of patents n semiconductor device structures and circuits. From 1987 to 1993, I consulted for clients in the semiconductor chip design and manufacturing industry. In 1993, I formed DynChip Corporation, a designer of FPGAs. I am currently Chairman of the Board of DynChip Corporation. I have obtained over my career more than 50 patents, probably closer to 60, most of which are on semiconductor device structures and some circuits.

In order to compare the attributes and properties of the Mori EEPROM cell described in U.S. patent 5,071,782 to the Vora EEPROM cell described in my patent application serial number 08/654,760, filed 5/29/96, I have done layouts of both cells using industry standard design rules and compared the cell size and array density for both cells. Exhibit A, page 1, attached, contains two tables that give the results of the comparison. The top table on page 1 gives the Mori and Vora cell sizes in square microns for one micron design rules in column 1 and, in column 2, the same cell sizes for 0.35 micron design rules.

The design rules used used in this study are given in Exhibit A, page 2. These design rules are industry standard and comprise a composite of the design rules used throughout the MOS integrated circuit industry. Each design rule is given a name or label as shown in the rightmost column on page 2.

The Mori cell layout using 1 micron design rules is shown on page 3 of Exhibit A, and the various design rules used to define each dimension are labeled on the layout of page 3 with the design rule name with a leader line to the dimension it defines.

The Vora cell layout using 1 micron design rules is shown in page 4 of Exhibit A, and the

various design rules used to defin ach dimension are labeled on the layout of page 4 with the design rule name with a leader line to the dimension it defines.

The Mori cell layout using 0.35 micron design rules is shown on page 5 of Exhibit A. The various dimensions are established by the same design rules as labelled in the 1 micron design rule Mori cell layout on page 3, but the values are different and are as established by the 0.35 micron design rule values given in the table on page 2.

The Vora cell layout using 0.35 micron design rules is shown on page 6 of Exhibit A. The various dimensions are established by the same design rules as labelled in the 1 micron design rule Vora cell layout on page 4, but the values are different and are as established by the 0.35 micron design rule values given in the table on page 2.

The Mori cell used in this study was the contactless cell shown in Figures 1a and 1b of his '782 patent having a buried source 32 brought to the surface at the end of the row at contact hole 32a and having a drain/bit line 34 formed in the substrate with a surface of the drain/bit line coincident with the surface of the substrate and with contact to the bit line 34 at the end of the row at contact window 34a. A floating gate FG formed from the poly 1 layer which is not self aligned was used in the layout. The floating gate of Mori requires a separate mask and separate alignment tolerances for the following reason. Mori's floating gate is formed by depositing poly 1 after the trenches are formed. After the poly 1 deposition, poly 1 covers the entire chip. If the same mask was used to define the floating gate on the poly 1 layer as is used to define the word line on the poly 2 layer, the poly 1 layer would be continuous between adjacent cells and would short them out rendering the array useless. Therefore, a separate mask is used to define

the limits of the poly 1 floating gate after poly 1 deposition and before poly 2 deposition. This mask for the floating gate requires alignment tolerances to the trench defined by design rule POLY 2-4 + POLY 2-3. The mask for the floating gate also requires alignment tolerances to the edge of the buried source bit line defined by design rule POLY 1-4.

In contrast, none of these alignment tolerances defined by POLY 2-4 + POLY 2-3 or POLY 1-4 is needed in the Vora cell because a mask is not used to form the floating gate in the Vora cell. Basically, in the Vora cell, a poly 0 layer is laid down after formation of the trenches, and then etched back to remove all horizontal components of poly 0 from the bottom of the trenches and any horizontal components at the top of the trenches. Because no mask is used for this, no alignment tolerances or wasted space is necessary in the Vora cell.

The Mori cell also uses an isolation barrier 15 between the buried source layer which is not used in the Vora cell thereby eliminating the alignment tolerances defined by design rules ISO-1 and ISO-2. Buried source layers in the Mori cell of adjacent rows each need to be spaced from the isolation barrier 15 by a distance equal to design rule ISO-1.

In contrast, the Vora cell does not use buried layer sources as the entire substrate has a doped layer which is grounded and serves as the source. Therefore, the wasted space defined by design rules ISO-1 and ISO-2 in the Mori cell is not wasted in the Vora cell.

All these structural differences between the Vora cell and the Mori cell result in substantial saving of chip area and much greater density for the Vora cell. The table of page 1 of Exhibit A shows that the Vora cell is slightly more than 3 times smaller than the Mori cell at 1

micron design rules and about 4.5 times smaller than the Mori cell at 0.35 micron d sign rules. These cell size differences result in an array density of 11.9 megabits per one square centimeter die size for the Vora cell at 1 micron and 69.44 megabits per square centimeter die at 0.35. In contrast, the Mori cell has a density of 3.57 megabits/sq. cm. at 1 micron (approximently 1/3 as dense as the Vora cell), and 15.55 megabits/sq. cm. at 0.35 microns (approximately 1/4 as dense as the Vora cell).

These substantial improvements arise from the use of a self aligned floating gate in the Vora cell and the elimination of the extra spacing between the buried source layers and the isolation barrier and the elimination of the trench to floating gate alignment tolerances in the Vora cell which need to be present in the Mori cell because of his lack of a self aligned floating gate.

Respectfully submitted,

Dated: June 9, 1998

Madhukar Vora

6/9/98

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231
on JUNE 9, 1998
(Date of Deposit)

Ronald Craig Fish, President
Ronald Craig Fish, a Law Corporation
Reg. No. 28,843

Cell Area in SQ. UM		
	1.0 UM Design Rules	0.35 UM Design Rules
Mori Patent	28	6.44
Vora Patent	8.4	1.44

Memory Density in Mega Bits per sq.cm		
	1.0 UM Design Rules	0.35 UM Design Rules
Mori Patent	3.57	15.55
Vora Patent	11.9	69.44

RULES TO LAYOUT MORI CELL AND VORA CELL(BY Madhu Vora dated 5/4/98)

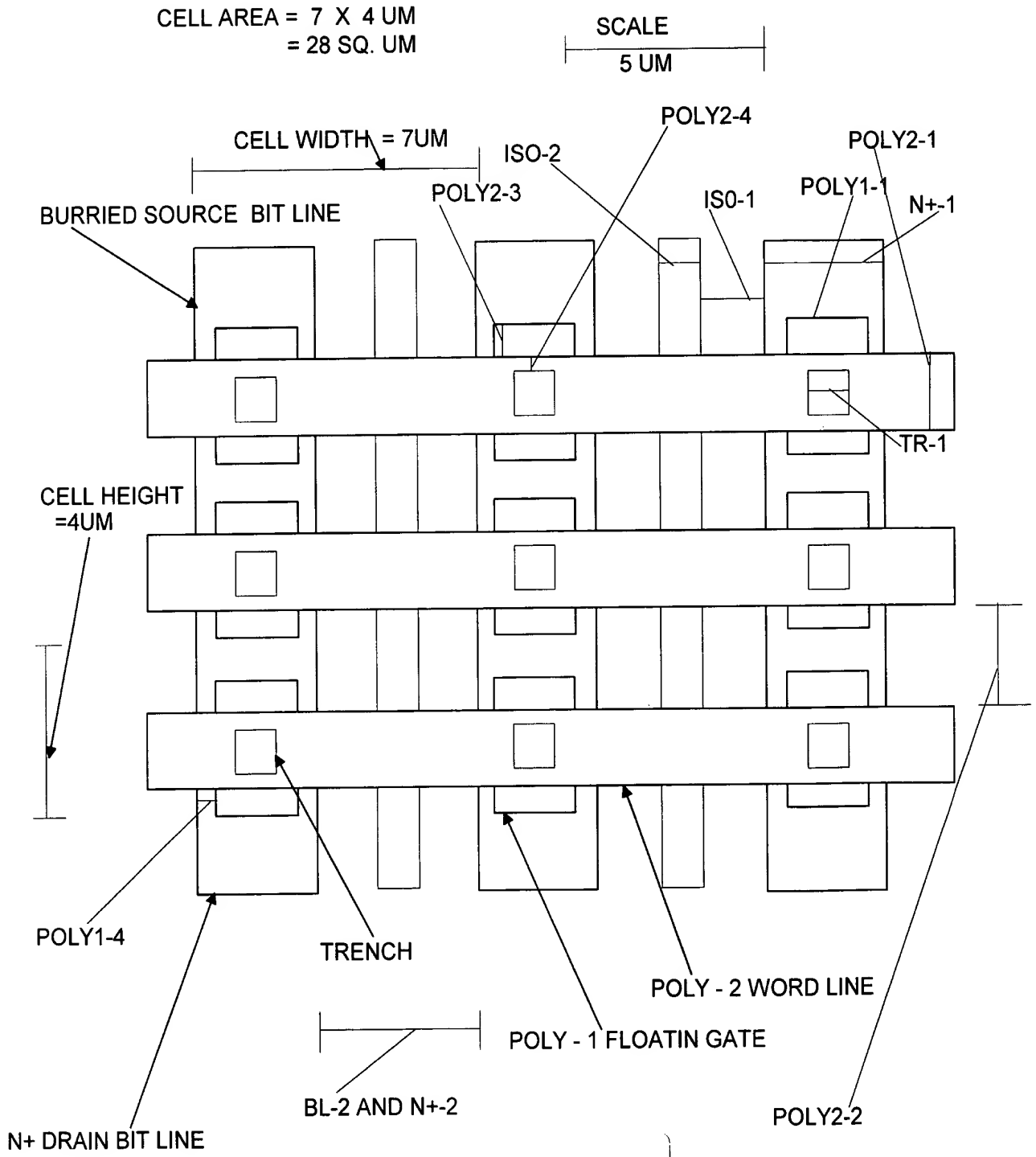
Minimum Dimentions	1.0 UM Design Rules	0.35 Design Rules	Design Rule Lable	
Buried lay r Mask				
Buried Layer Width	1.00	0.4	BL-1	
Buried Layer to Buried layer space	4.00	5.40	BL-2	Note#1
Buried Layer Lateral Diffusion	1.00	1	BL-3	
ISO Mask				
Buried layer to Iso layer space	0.50	1.5	ISO-1	
Iso Layer Width	1	0.4	ISO-2	
			ISO-3	
N+ Mask				
N+Layer(Drain Bit Line) Width	1	0.4	N+-1	
N+Layer(Drain Bit Line) to N+Layer Space	1	0.5	N+-2	
Under lap of N+ on BL	0.5	0.2	N+-3	
Trench Mask				
Width	1	0.4	TR-1	
Space	1	0.4	TR-2	
Underlap of trench inside of BL	0.5	0.2	TR-3	
Poly-1 Mask				
Width	1	0.35	POLY1-1	
Space	1	0.35	POLY1-2	
Edge of Poly-1 mask to the edge of trench	0.5	0.2	POLY1-3	
Poly1 to edge of N+ bitline	0.5	0.2	POLY1-4	
Poly-2 Mask				
Width	1	0.35	POLY2-1	
Space	1	0.35	POLY2-2	
Underlap of Edge pf Poly-2 inside Poly-1	0.5	0.2	POLY2-3	
Poly2 to trench	0.5	0.2	POLY2-4	

to BL space= Lateral Diffusion X 2 +BL to ISO spacing X 2 +ISO width

EXH. A, p. 2

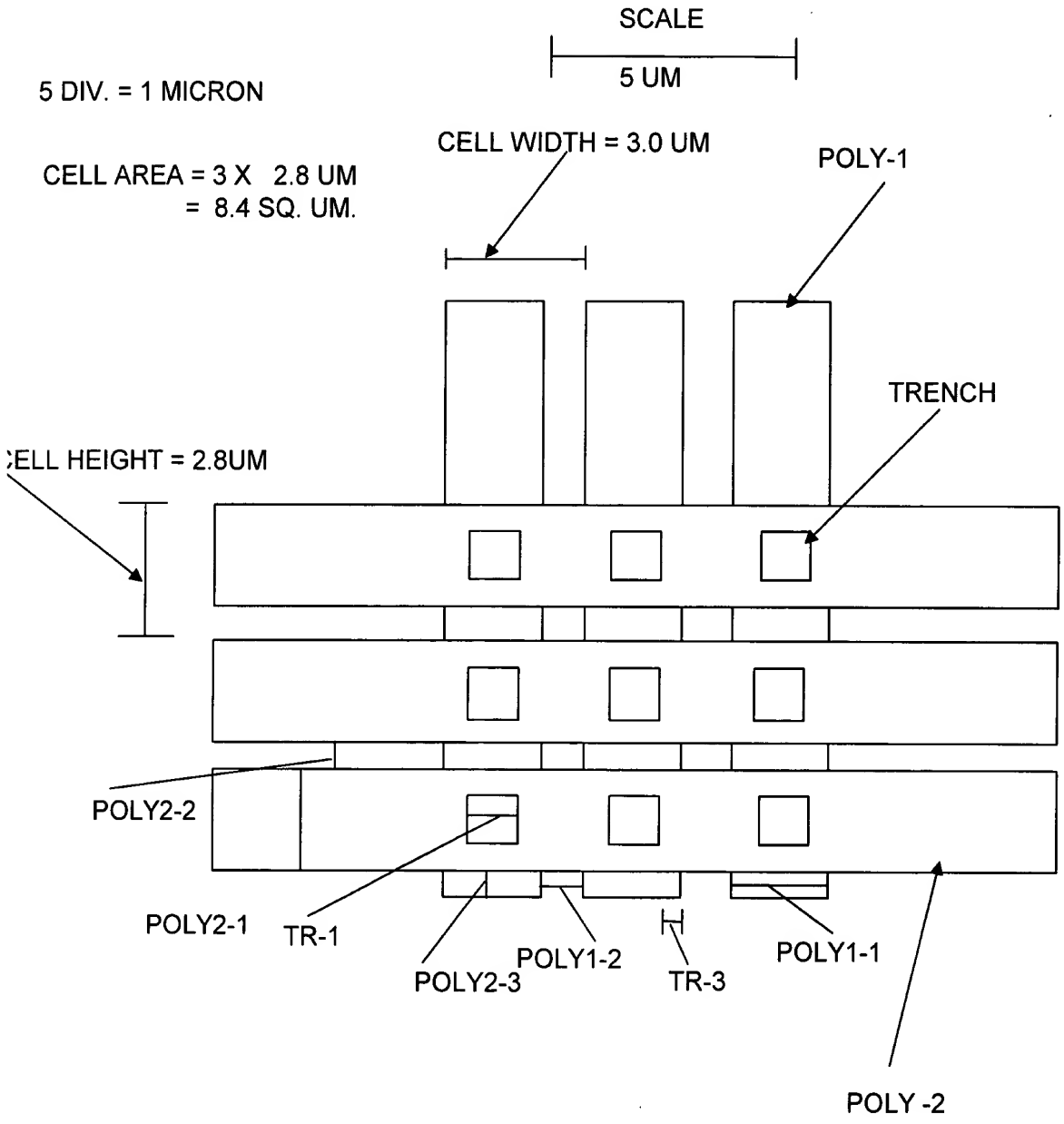
MORI CELL LAYOUT BY MADHU VORA 6/4/98

1 UM DESIGN RULES



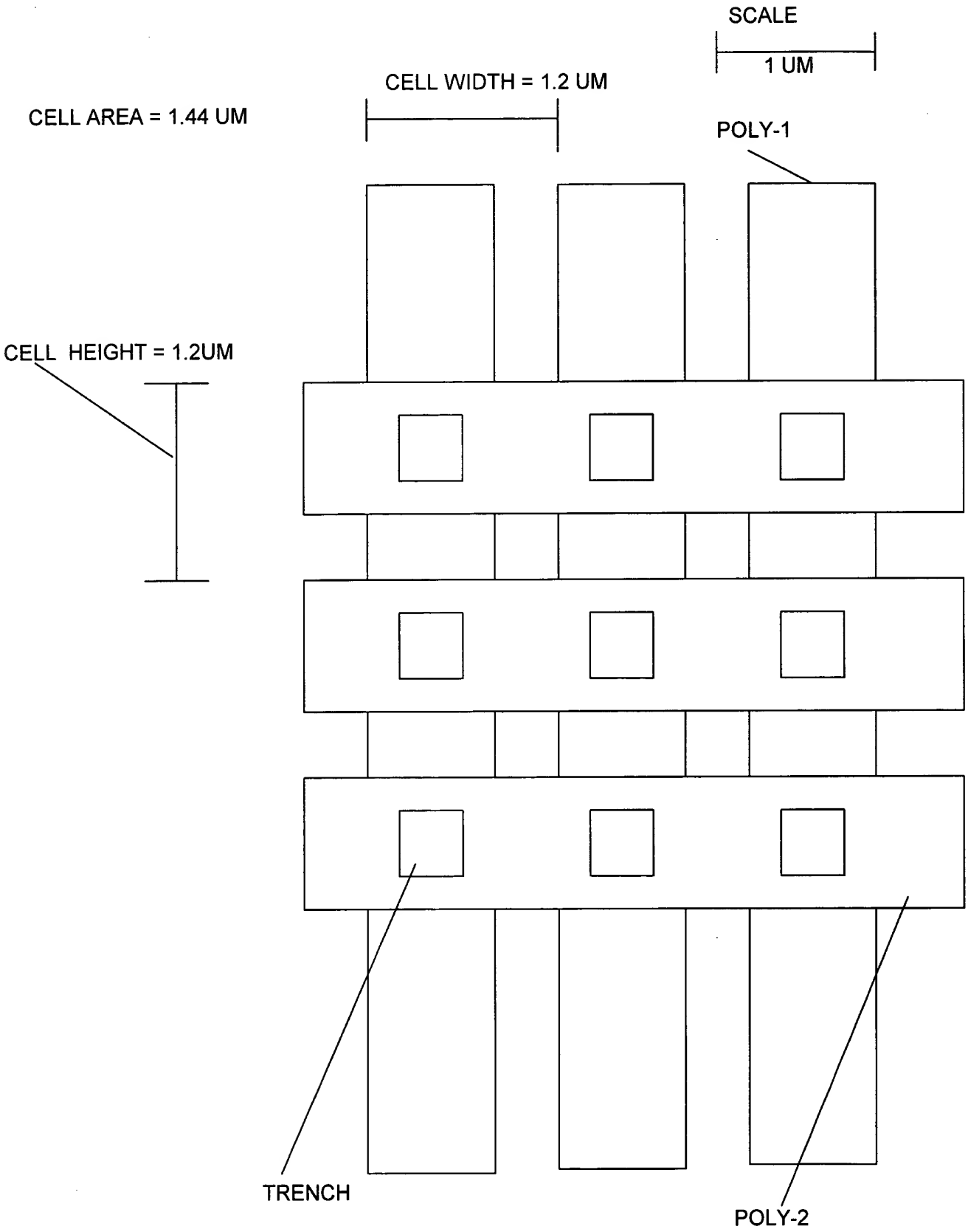
VORA CELL LAYOUT BY MADHU VORA 6/4/98

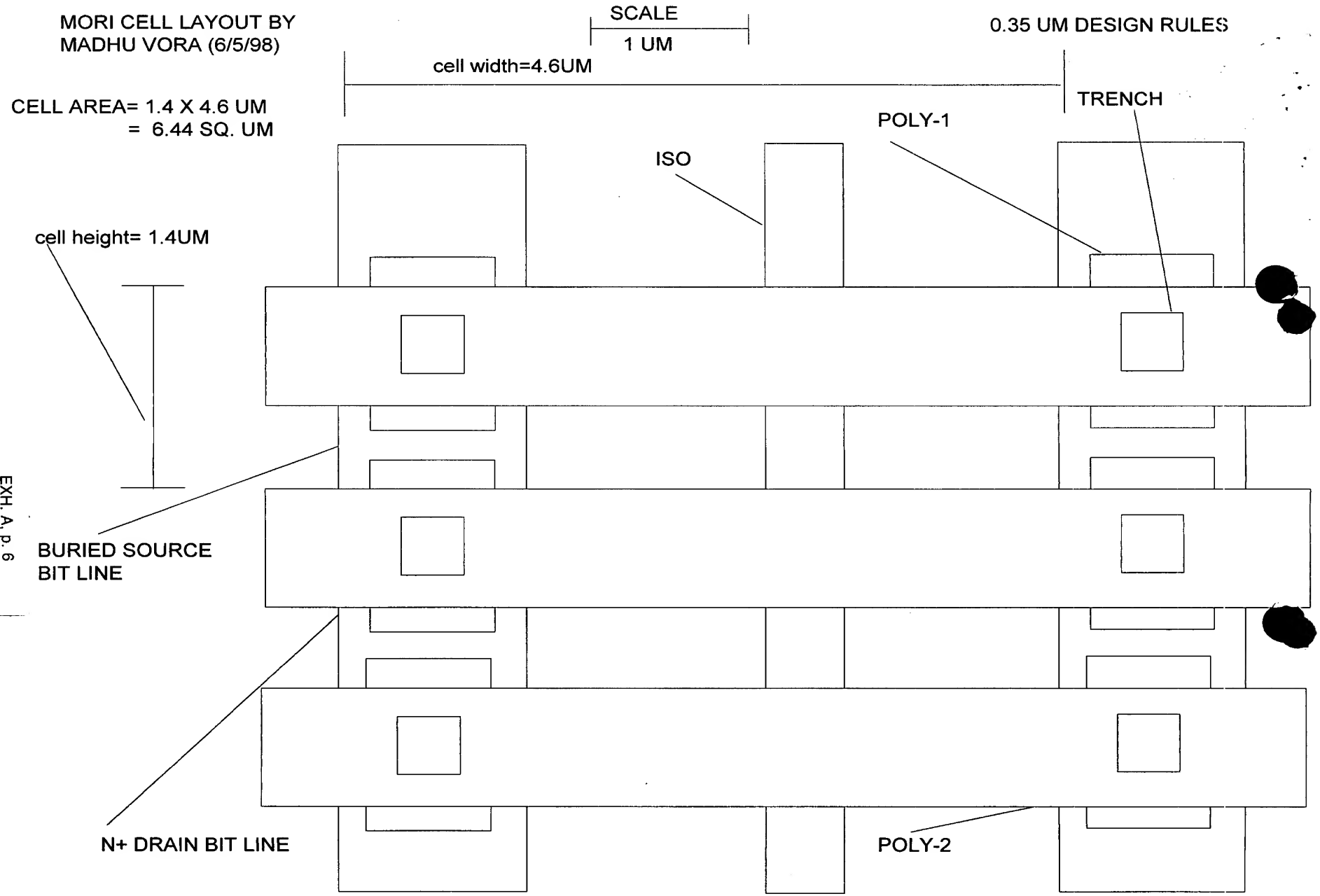
1 UM DESIGN RULES



0.35UM DESIGN RULES

VORA CELL LAYOUT BY MADHU VORA (6/5/98)




MORI CELL LAYOUT BY
MADHU VORA (6/5/98)
SCALE
1 UM
0.35 UM DESIGN RULES
cell width=4.6UM
CELL AREA= 1.4 X 4.6 UM
= 6.44 SQ. UM
TRENCH
POLY-1
ISO
cell height= 1.4UM
BURIED SOURCE
BIT LINE
N+ DRAIN BIT LINE
POLY-2

Use of Poly Layers in Mori and Vora Patents

	POLY-0	POLY-1	POLY-2
MORI PATENT	Does not exist	Floating Gate	Word Line
VORA PATENT	Floating Gate	Word Line	Bit Line